

# **An Open Architecture for an Embedded Signal Processing Subsystem for the Fire Control System MK 92 Combined Antenna System's Radar**

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## **Abstract**

This briefing describes the effort to implement advanced embedded signal processing for the MK 92 Fire Control System (FCS) Combined Antenna System's (CAS) search DSP with a focus on Open Architecture. The end goal of this effort was to achieve a low cost open architectural reconfigurable and generic DSP. A team of both US and international partners was assembled from LMC, INDRA Sistemas, and CSPI. LMC acted as the system design agent with responsibility for the definition of the COTS architecture, technical requirements and the MK 92 FCS integration. Indra's responsibility was for the software development that included design, implementation and test of embedded DSP. CSPI responsibilities included the development of the radar real-time hardware and interfaces for MK 92.

The goals of this effort were to:

- Develop requirements and open architecture implementation
  - Develop Matlab model of the signal processor
  - Analyze the processing requirements based on benchmarks from actual COTS hardware
  - Compare performance, size and cost with existing embedded COTS processor architectures
- Develop methodology for the radar processing algorithms
  - Object-oriented software design
  - Utilize actual hardware to develop and measure real-time algorithms
  - Matlab simulation for test vector generation and verification
- Develop a flexible interface concept
  - Develop hardware interfaces and software to legacy interfaces while still maintaining an open architecture approach

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- Maintain the ability to program the DSP through the use of industry standard APIs and Portability Standards, such as VSIPL and MPI
- Integrate the subsystem
  - Demonstrated tactical system operation using the MK 92 Radar Stimulator and Scenario Scripting equipment. The ability to provide a realistic stimulus to the RGSD aided in the test and evaluation of the DSP

Key results associated with the usage of Open Hardware and Software COTS solutions are presented. Specific metrics of merit are used to compare the MK 92 COTS version with its previous legacy implementation, outlining the benefits of the subject approach for the implementation of an advanced tactical radar:

- Cost of Development
- Concurrent Engineering to minimize Development Time
- Power & Size reduction
- Recurring Cost
- Flexibility & Performance
- Radar Upgrade
- Future Technology Upgrade
- Supportability & Diminishing Manufacturing Sources

# **An Open Architecture for an Embedded Signal Processing Subsystem**

*7th Annual Workshop on High Performance Embedded  
Computing*

*MIT Lincoln Laboratory  
23-25 Sept 2003*

**Stephen F. Shank**  
**Principal Member**  
**Engineering Staff**



# Project Summary



- ***The Objectives:***

- ***Utilize High Performance Embedded Computing To Replace Legacy Signal Processor Equipment In Future Radar Programs***
- ***Assemble A Project Team To Define, Develop And Code The Key Functions Of The Open Architecture Digital Processor***
- ***Demonstrate A Prototype In 15 Months***

- ***The Players:***

- ***Lockheed Martin – Radar Design Agent And System Integrator***
- ***INDRA –Spanish Radar Company And Software Developer***
- ***CSPI - COTS Hardware Supplier And Investment Partner***
- ***VMETRO - COTS Data Recorder***
- ***Primagraphics - COTS Display***

- ***Lockheed Martin Tasks:***

- ***Develop The Hardware / Software Architecture***
- ***Define Target Radar Characteristics And Provide Specifications, Matlab Models, Interface Requirements, Etc.***
- ***Conduct Integration And Test Activities***

- ***INDRA Tasks:***

- ***Design, Develop, Code, And Test Key Functions Of The COTS DSP***
- ***Support Integration & Test***

- ***CSPI Tasks:***

- ***Provide Training To INDRA***
- ***Provide Hardware And Software Development Environment***
- ***Develop Radar Interface Boards***
- ***Provide Development Support***

- ***VMETRO:***

- ***Provide Recorder Equipment***

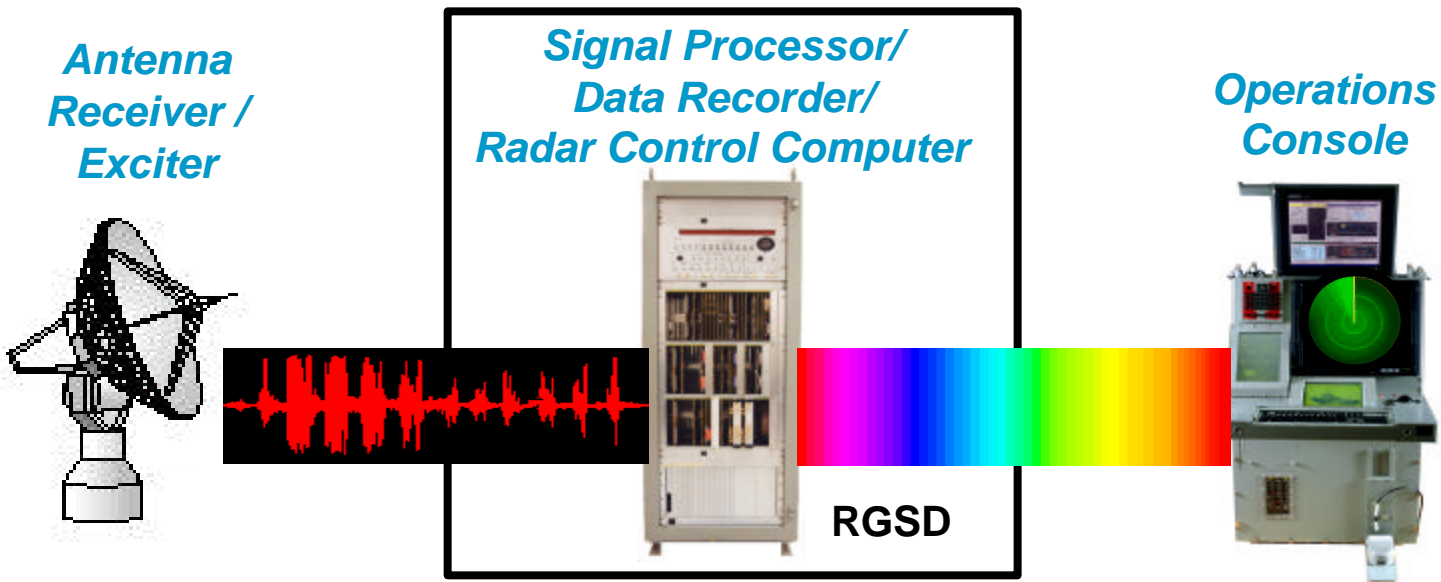
- ***Primagraphics:***

- ***Provide Radar Display Equipment***

**International Development Team Assembled**

# Project Plan:

## Reconfigurable Generic Search Radar Digital Signal Processor (RGSD)



- ***Define radar characteristics, specifications, Matlab Models and system interfaces***
- ***Develop a flexible hardware / software architecture***
  - *Software is reusable and scalable*
  - *Hardware is scalable and refreshable*
- ***Conduct Integration and Test activities in radar test bed***

**Demonstrate RGSD in a Legacy Radar in 15 months**

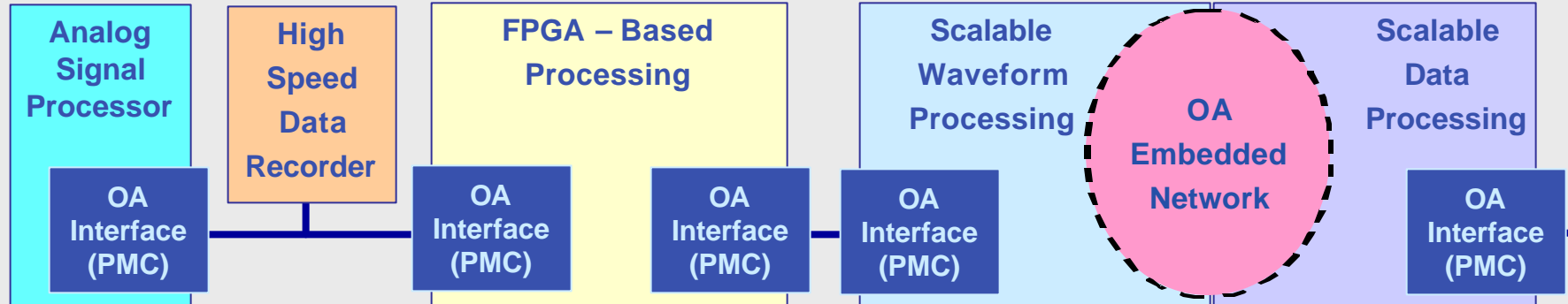
# Open Architecture Digital Processor



## Digital Processor (DP) Subsystem

ASP/ DSP / RCP Application Software

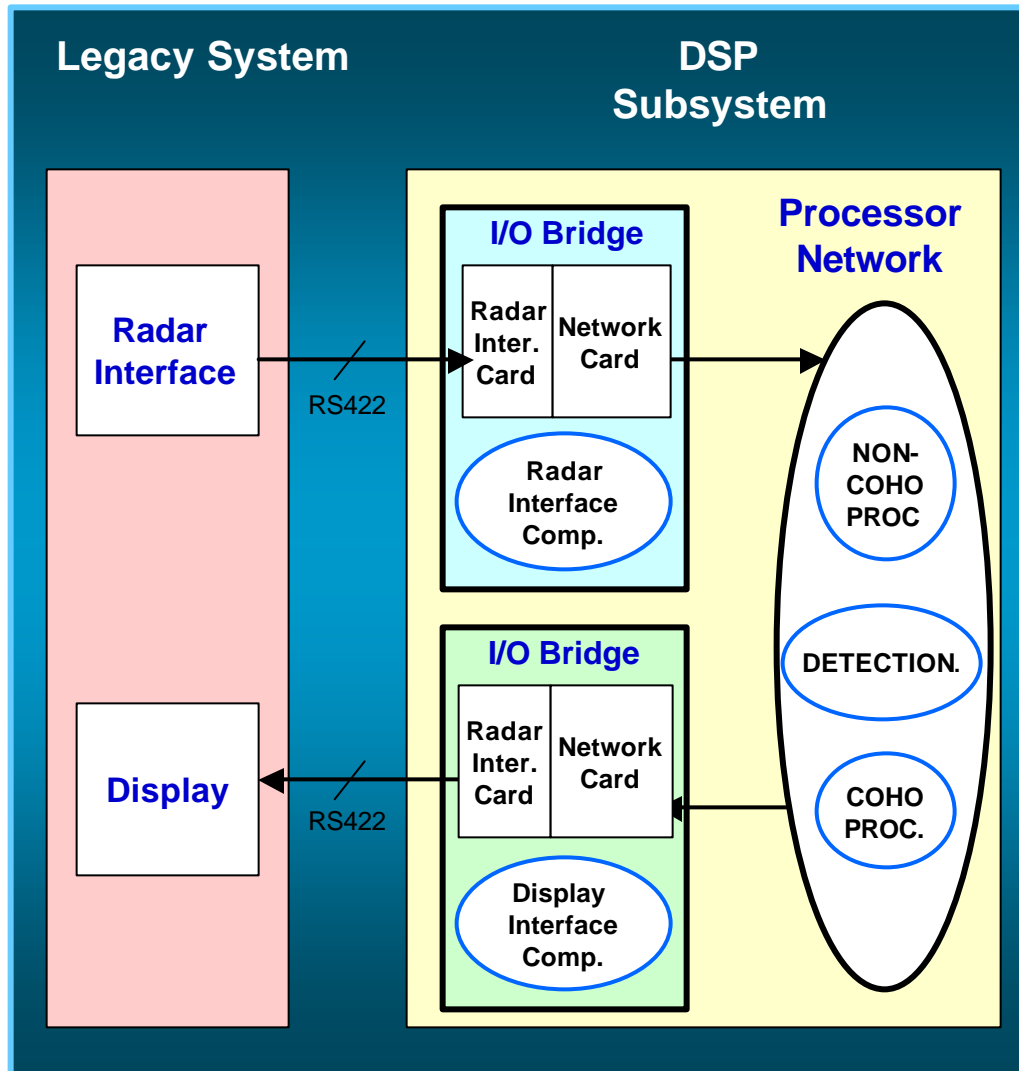
API, Common Services, OA Middleware (MPI & VSIPL)



- **Software - Object-Oriented, C/C++**
- **Requirements Management – Telelogic DOORS**
- **OO Modeling – Rational Suite (Rose)**
- **Configuration Management – Rational ClearCase**
- **Integration & Test – VxWorks Tornado 2**
- **Standard API, OA Middleware**
  - **Open Message Passing Software**
    - **MPI & TCP/IP**
  - **Standard Signal Processing Libraries**
    - **VSIPL**
  - **Support for Open Architecture Standards**
    - **VME 64, Fibre Extreme, PCI/PMC capable, Myrinet**

**Independent, Scalable, Reusable Software**

# RGSD Development Methodology

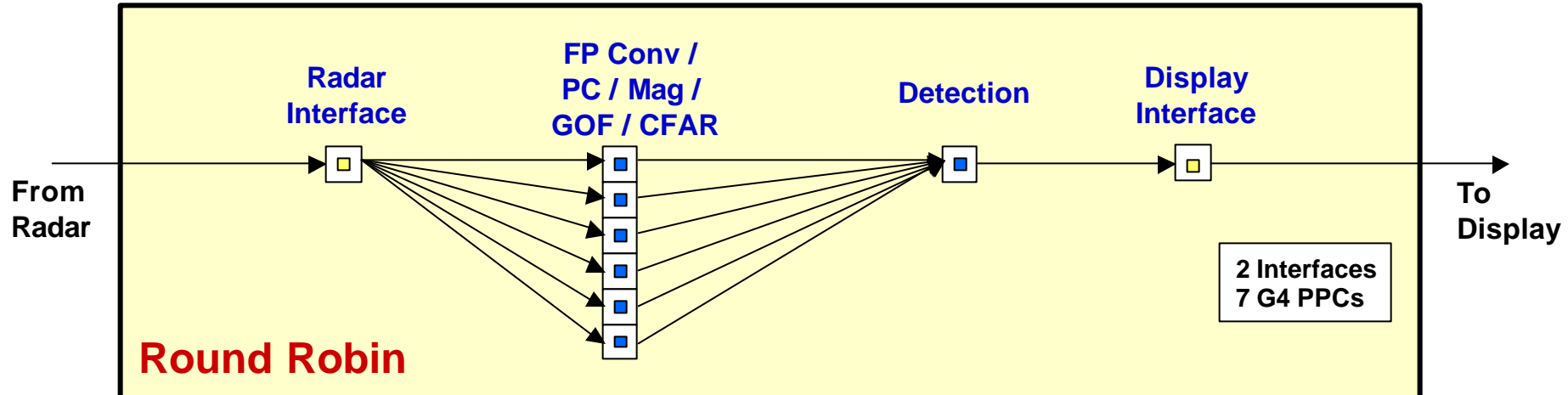
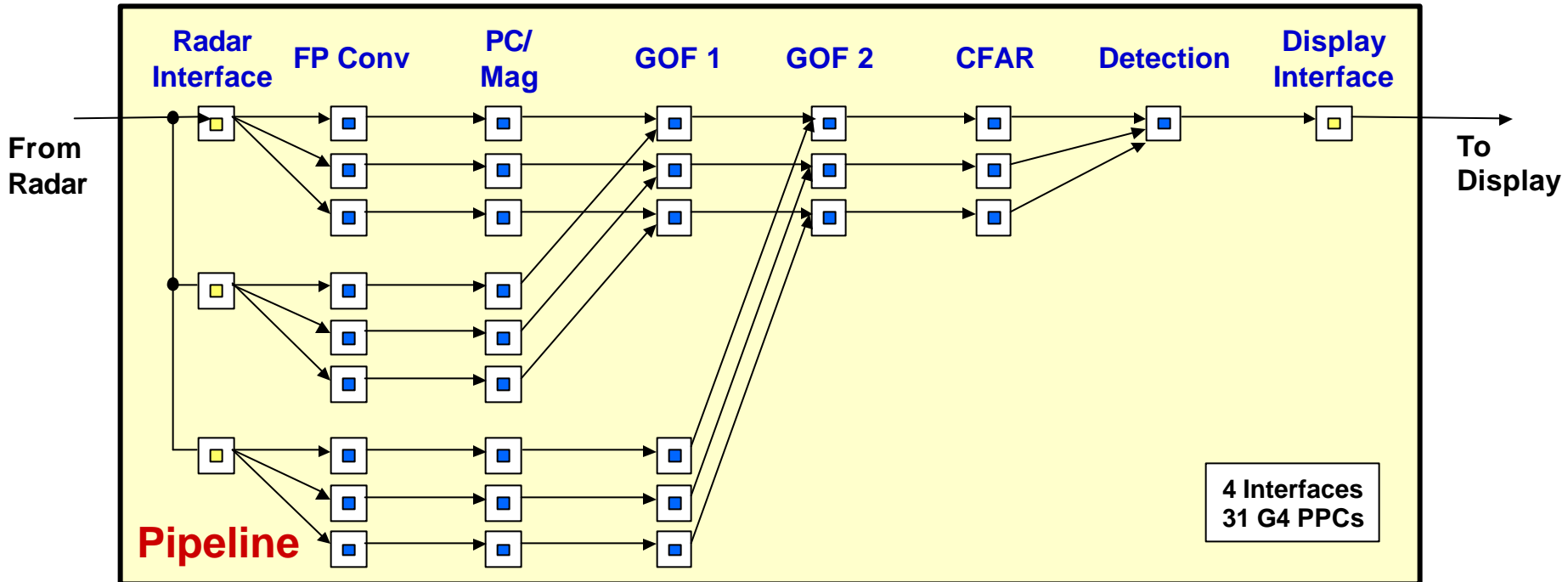


- **Determine Processing Requirements for Waveform Suite**
- **Partition Processing Requirements into 5 Functional Groups**
  - Radar Interface Component
  - Display Interface Component
  - Coherent Waveform Processing
  - Non-Coho Waveform Processing
  - Detection
- **Map Algorithm Functionality to Processor Configuration**
- **Identify Potential Risk Areas**
  - Processing Intensive (e.g. Match Filtering)
  - I/O Intensive
- **Design Software using**
  - High Level Language (C/C++)
  - Common Application Programmer's Interfaces (API) such as MPI/VSIP for scalability and portability
- **Validate Software against MatLab Hardware Model**

# Non Coherent Processing Architecture

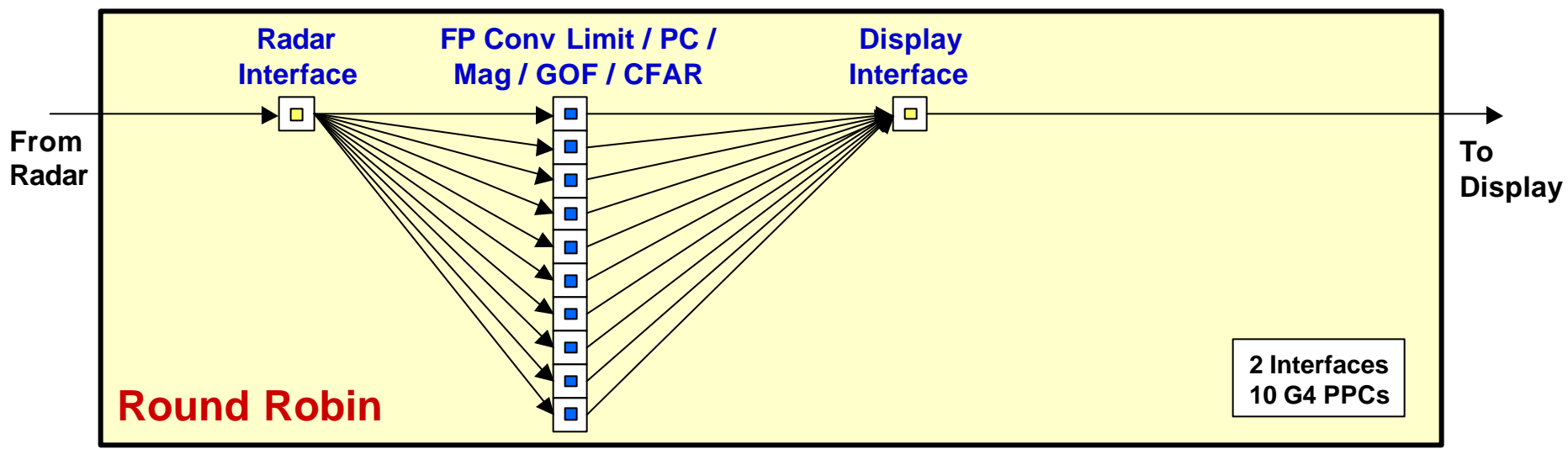
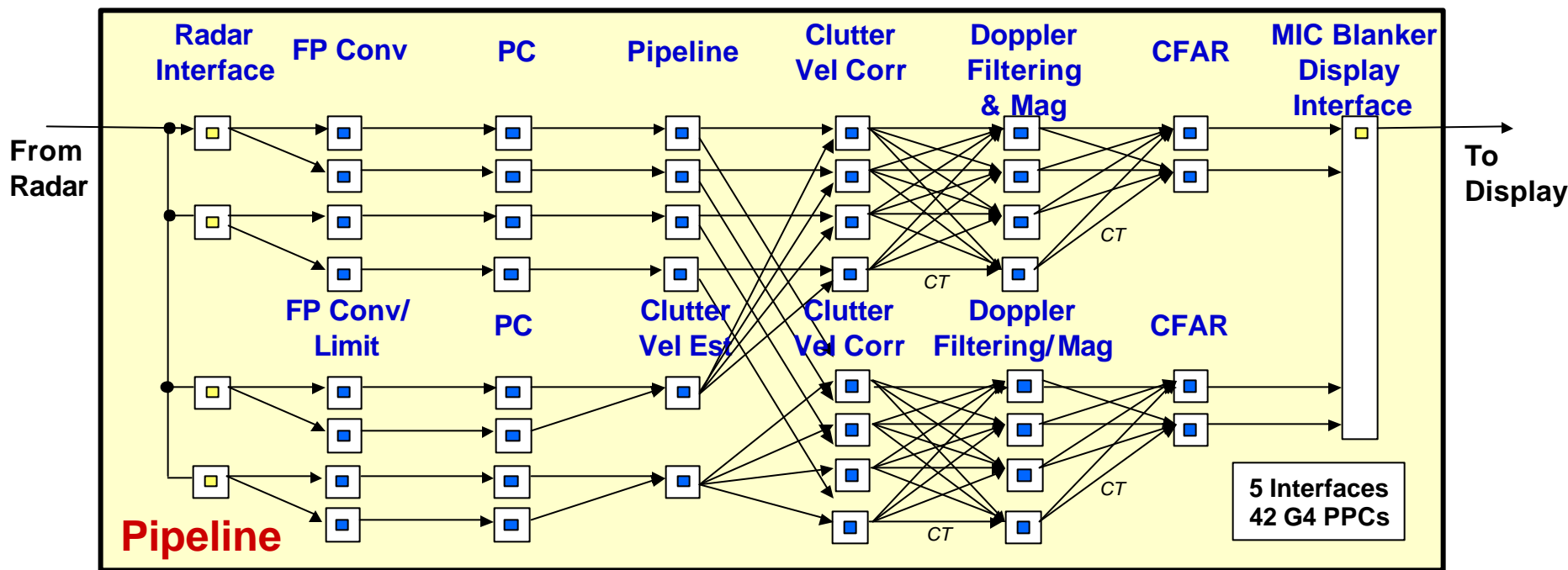


-Two Options:

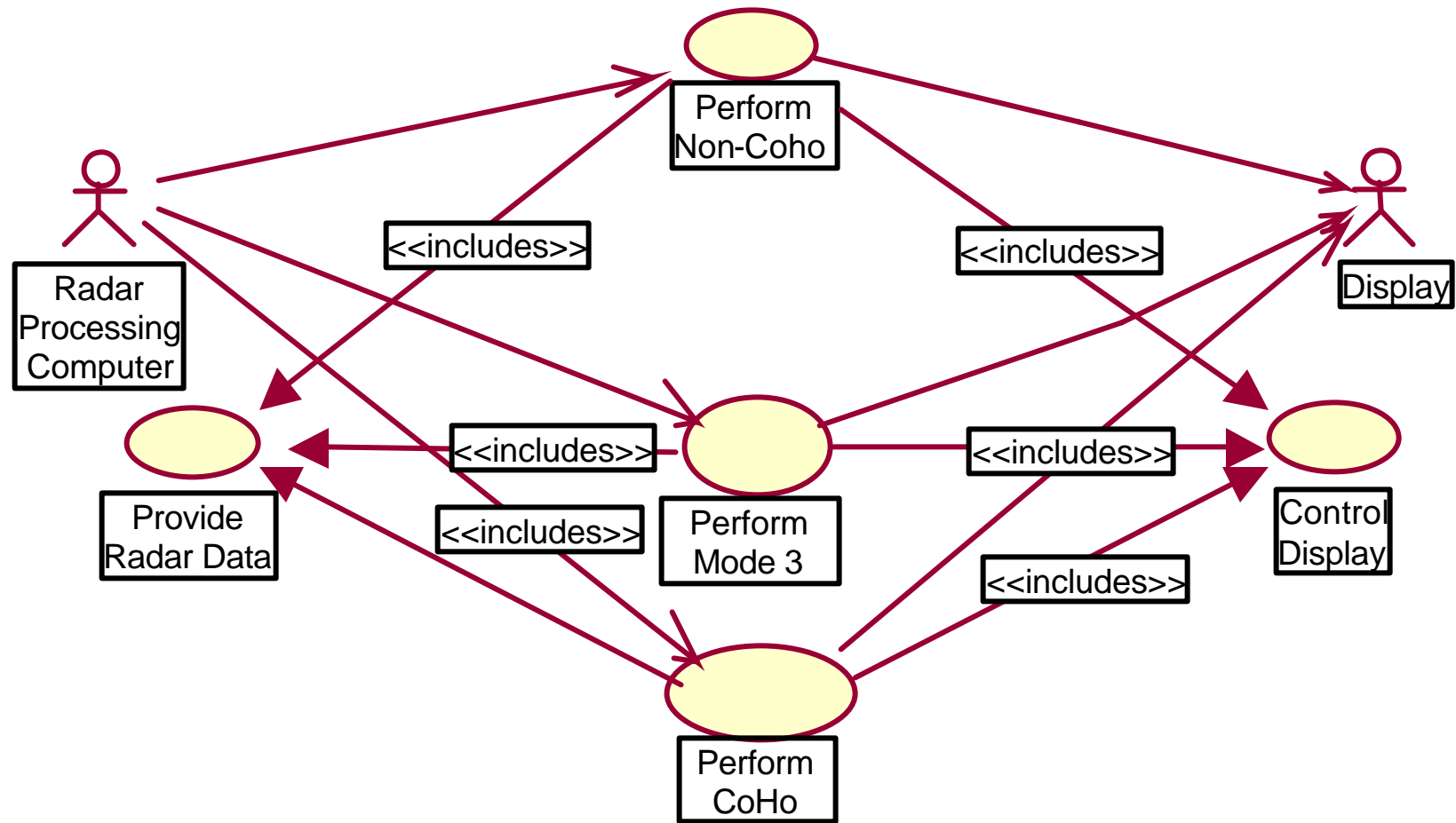


# Coherent Processing Architecture

-Two Options:



# Top Level RGSD Use Case Diagram



Visual Modeling maximizes the team's development productivity

# Architecture Comparison



Cost Drivers

Latency ( $\mu$ s)

Waveform	Estimate Pipeline	Estimate Round Robin	Actual Round Robin
Non-Coho 1	7,140	5,540	2,270
Non-Coho 2	3,570	3,710	1,970
Non-Coho 3	3,570	1,920	900
Coho 1	14,480	19,760	15,620
Coho 2	15,360	22,130	18,210

Number of PPCs (G4)

Waveform	Estimate Pipeline	Estimate Round Robin	Actual Round Robin
Non-Coho 1	31	7	3
Non-Coho 2	25	5	5
Non-Coho 3	11	3	2
Coho 1	42	9	9
Coho 2	35	10	10

Processing (%)

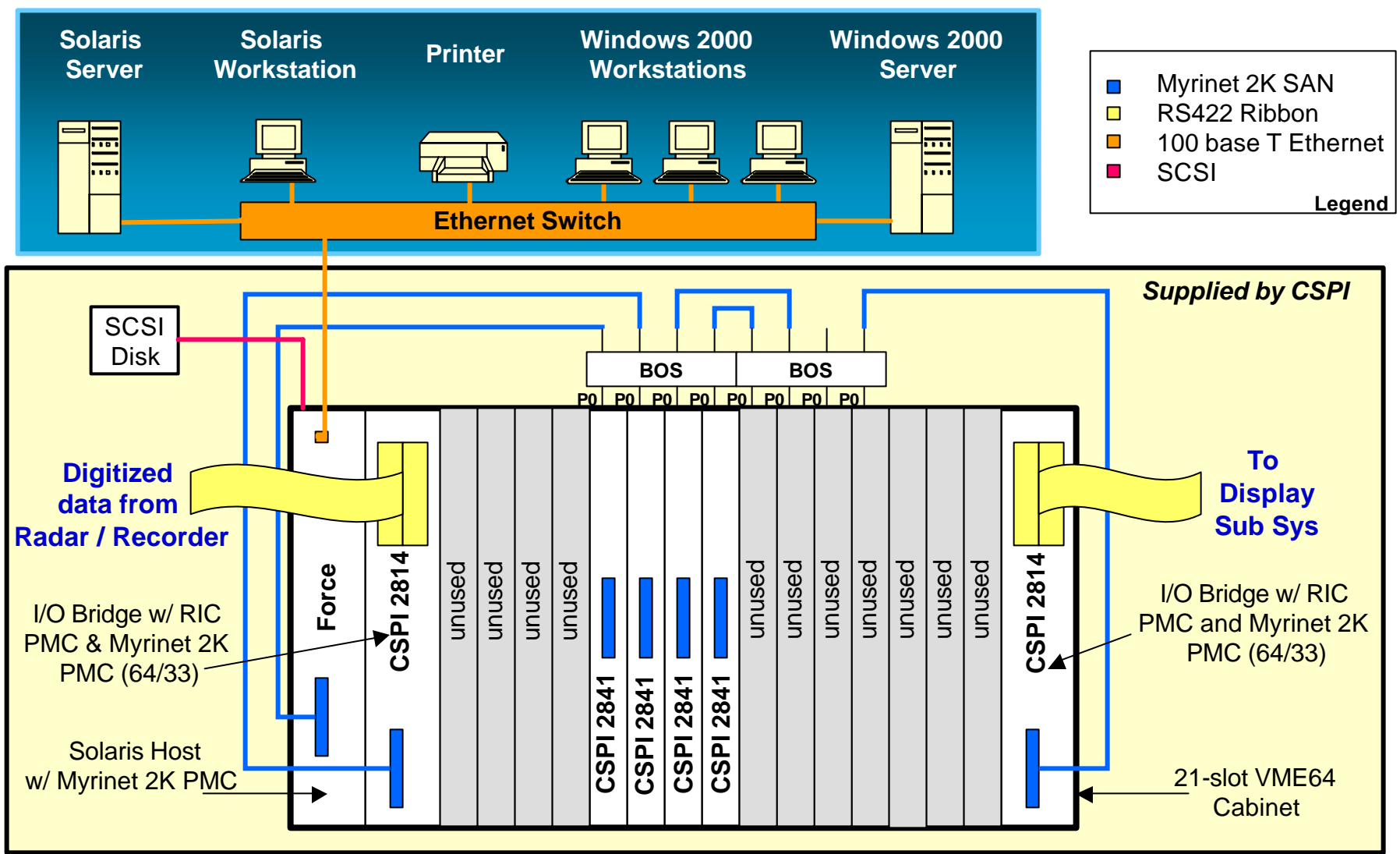
Waveform	Estimate Pipeline	Estimate Round Robin	Actual Round Robin
Non-Coho 1	49	96	89
Non-Coho 2	62	94	87
Non-Coho 3	50	88	71
Coho 1	58	91	89
Coho 2	55	90	87

I/O (%)

Waveform	Estimate Pipeline	Estimate Round Robin	Actual Round Robin
Non-Coho 1	51	4	11
Non-Coho 2	38	6	13
Non-Coho 3	50	12	29
Coho 1	42	9	11
Coho 2	45	10	13

Round Robin Meets Requirements with Fewer Processors

# RGSD Development System Configuration



Open Architecture with Scalable Performance

# Dual Radar and Display Interface



- *Provides in a PMC Form Factor*
  - *RS-422 Interface to Radar Processor and Display console*
  - *User programmable CPLD*
  - *High performance (64/66) PCI controller providing a high bandwidth/low latency connection between the CPLD and the PMC connectors*

## ***Radar Interface Personality***


- ***Buffers and packetizes I / Q data***
- ***DMA's packets to host memory for access by MPI***
- ***Supports Test Data Injection***
- ***Round-Robin queuing of radar data to destination software component based on waveform***

## ***Display Interface Personality***

- ***DMA's data from host memory***
- ***Sorts packets***
- ***Buffers packet in preparation for display***
- ***Restores time characteristics for proper display***
- ***Generates output signals (data and synchronization) to display console***

**Hi-Performance Programmable Interface**

# Project Summary

- 
- ***RGSD Prototype was successfully integrated at Lockheed Martin***
    - *System Integration and Test completed in less than three weeks*
      - *Successful use of Matlab model of legacy hardware substantially reduced I&T effort*
  - ***RGSD will be leveraged for future radar programs***
    - *Addresses production cost and Diminishing Material Supply (DMS) issues of current systems by replacing legacy equipment with COTS*
    - *Software based OA design provides the ability to enhance or modify system operation without the need for major redesigns*
  - ***Project validated benefits of High Performance Embedded Computing***
    - ***Reduces Cost for:***
      - *Development effort*
      - *Acquisition / Life Cycle Cost*
    - ***Provides:***
      - *Scalable and Reusable Signal Processing Software applicable to a wide variety of radar applications*

**Cost Effective use of OA Standards for Real Time Radar Applications**